

WHAT IS CLAIMED IS:

1                   1.       A delay locked loop (DLL) for compensating for a skew in a  
2 synchronous dynamic random access memory, comprising:  
3                   a delay model means for delaying an external clock signal by the skew to  
4 generate a delayed clock signal;  
5                   a control means, in response to the external clock signal and the delayed clock  
6 signal, for generating control signals, wherein the control signal includes a control clock  
7 signal, a delayed control signal, a replication signal and a replication enable signal;  
8                   a first voltage controlled oscillation means, in response to the control clock  
9 signal and the delayed control signal, for generating a measurement oscillating signal;  
10                  a second voltage controlled oscillation means, in response to the replication  
11 signal and the replication enable signal, for generating a replication oscillating signal;  
12                  a first means, in response to the measurement oscillating signal and the  
13 replication oscillating signal, for generating a DLL clock, signal; and  
14                  a second means for comparing a phase difference between the DLL clock  
15 signal and the external clock signal to generate a voltage control signal, wherein time periods  
16 of the measurement oscillating signal and the replication oscillating signal are changed by the  
17 voltage control signal.

1                   2.       The delay locked loop as recited in claim 1, wherein the control clock  
2 signal is enabled to a high level from a first rising edge to a second rising edge of the external  
3 clock signal.

1                   3.       The delay locked loop as recited in claim 2, wherein the delayed  
2 control signal is enabled to a low level from a first rising edge to a second rising edge of the  
3 delayed clock signal.

1                   4.       The delay locked loop as recited in claim 3, wherein the measurement  
2 oscillating signal is toggled while both the control clock signal and the delayed control signal  
3 are enabled.

1                   5.       The delay locked loop as recited in claim 4, wherein the first voltage  
2 controlled oscillation means includes:  
3                   a NOR gate have an input terminal receiving the delayed control signal;

4 a delay control unit for delaying an output signal of the NOR gate in response  
5 to the voltage control signal;  
6 a NAND gate for NANDing the control clock signal and an output signal of  
7 the delay control unit;  
8 a delay unit for delaying an output signal of the NAND gate, wherein an  
9 output signal of the delay unit is feedback to another input terminal of the NOR gate; and  
10 an inverter for inverting the output signal of the NAND gate to generate the  
11 measurement oscillating signal.

1 6. The delay locked loop as recited in claim 4, wherein the second  
2 voltage controlled oscillation means includes:

3 a NOR gate having an input terminal receiving the replication signal;  
4 a delay control unit for delaying an output signal of the NOR gate in response  
5 to the voltage control signal;  
6 a NAND gate for NANDing the replication enable signal and an output signal  
7 of the delay control unit;  
8 a delay unit for delaying an output signal of the NAND gate, wherein an  
9 output signal of the delay unit is feedback to another input terminal of the NOR gate; and  
10 an inverter for inverting the output signal of the NAND gate to generate the  
11 replication oscillating signal.

1 7. The delay locked loop as recited in claim 4, wherein the first means  
2 includes:

3 a plurality of delay units for shifting a low level of the delayed control signal  
4 to corresponding nodes in response to the measurement oscillating signal;  
5 a plurality of registers for storing shifted low levels on the nodes; and  
6 a delay replication unit, in response to an output signal of the registers, for  
7 shifting the replication signal according to the replication oscillating signal to generate the  
8 DLL clock signal.

1 8. The delay locked loop as recited in claim 7, wherein each register  
2 includes:

3 a first inverter for receiving a voltage level of corresponding node to put an  
4 inverted signal;

5 a transmission gate for transmitting inverted signal in response to the control  
6 clock signal;  
7 a storage unit for storing the an output signal for the transmission gate; and  
8 a second inverter for inverting an output signal of the storage unit.

1 9. The delay locked loop as recited in claim 1, wherein the second means  
2 includes:

3 a second delay mode for delaying the DLL clock signal by the skew to  
4 generate a comparison clock signal;  
5 a phase detector for comparing the phase difference to generate an up pulse  
6 signal and a down pulse signal according to the phase difference;  
7 a charge pump decreasing and increasing the voltage level of the voltage  
8 control signal in response to the up pulse signal and the down pulse signal; and  
9 a filter for removing high-frequency noise of the voltage control signal.

1 10. The delay locked loop as recited in claim 9, wherein the down pulse  
2 signal is generated if the comparison clock signal precedes the external clock signal, thereby  
3 decreasing the voltage level of the voltage control signal.